# APPA2.01 SGW111X BLE Module Power Mode Configuration

*April 2020 V1.1*

## Introduction

The SGW111X BLE Module supports the following power modes:

1. System ON mode
   a. Normal Voltage mode
      i. LDO Configuration
      ii. DC/DC Configuration
   b. High Voltage mode
      i. LDO Configuration
      ii. DCDC Configuration
2. System OFF mode
   a. Internal DETECT signal reactivation
   b. Internal ANADETECT signal reactivation
   c. Internal SENSE signal reactivation
   d. Hardware RESET signal reactivation
   e. Valid USB voltage reactivation

This document outlines the configuration process of each power mode.

## Power Mode Configuration

1. <u>System ON mode</u>

   SGW111X is default at System ON mode, and also after every power reset. All functional blocks, such as CPU or peripherals, can be in IDLE or RUN mode, depending on the configuration setting of the software and the state of the application execution.

   SGW111X's design is based on the Nordic nRF52840 SoC, with two internal supply regulator stages. Each regulator stage has Low-dropout regulator (LDO) and Buck regulator (DC/DC).

   *a. Normal Voltage Mode (VCC = 1.7V to 3.6V)**

   Supply voltage is connected to both the VCC and VCCH pins, with the maximum supply voltage being 3.6V. Circuit configuration per Figure 1.

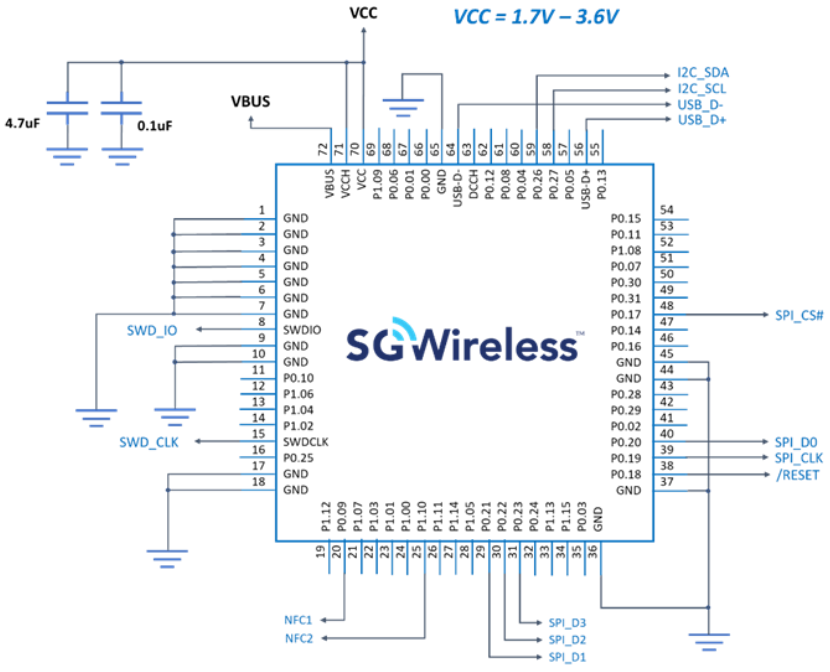


***Figure 1:*** *Normal Voltage Mode Circuit Configuration*

i. LDO Configuration
By default, the LDO regulators are enabled and the DC/DC regulators are disabled.

ii. DC/DC Configuration
DC/DC configuration is enabled with function command:

```
sd_power_dcdc_mode_set(NRF_POWER_DCDC_ENABLE);
```

*Remarks:
1. When a DC/DC converter is enabled, the LDO for the corresponding regulator stage will be disabled. The LC filter in REG1 stage is designed in SGW111X.
2. Using a DC/DC regulator reduces the overall power consumed, and offers higher efficiency than an LDO regulator.

*a. High Voltage Mode (VCCH ≤ 5.5V)†*
Supply voltage is only connected to the VCCH pin, and both internal supply regulator stages will be enabled. The output of the first stage regulator can be used to support external circuitry through the VCC pin. Maximum supply voltage of VCCH is 5.5V.

i. LDO Configuration
By default, the LDO regulators are enabled and the DC/DC regulators are disabled. Circuit configuration per Figure 2.

ii. DC/DC Configuration
DC/DC configuration is enabled with function command:

```
sd_power_dcdc_mode_set(NRF_POWER_DCDC_ENABLE);
sd_power_dcdc0_mode_set(NRF_POWER_DCDC_ENABLE);
```

Circuit configuration per Figure 3.

† Remarks:
1. For DC/DC operation at REG0 stage, the external inductor L1 is a must for connecting the DCCH and VCC pins. If it is not present, the DC/DC regulator will be disabled as the filter will inhibit regulator operation.
2. When a DC/DC converter is enabled, the LDO for the corresponding regulator stage will be disabled.

3. System OFF mode
System OFF mode is a deep sleep mode in which the system's core functionalities are shut down and all ongoing tasks are terminated. To put SGW111X in System OFF mode, write into the POWER register interface:

| Register | Offset | Value | Description |
|---|---|---|---|
| System OFF | 0x500 | 1 | Enable System OFF mode |

To reactivate SGW111X, use one of the following five methods. The system is reset upon reactivation.

a. Internal DETECT signal, optionally generated by the GPIO peripheral.
The target GPIO pin can be configured to generate the DETECT signal with the SoftDevice function:

```
nrf_gpio_cfg_sense_input(PIN_NUMBER,NRF_GPIO_PIN_PULLUP,NRF_GPIO_PIN_SENSE_LOW)
```

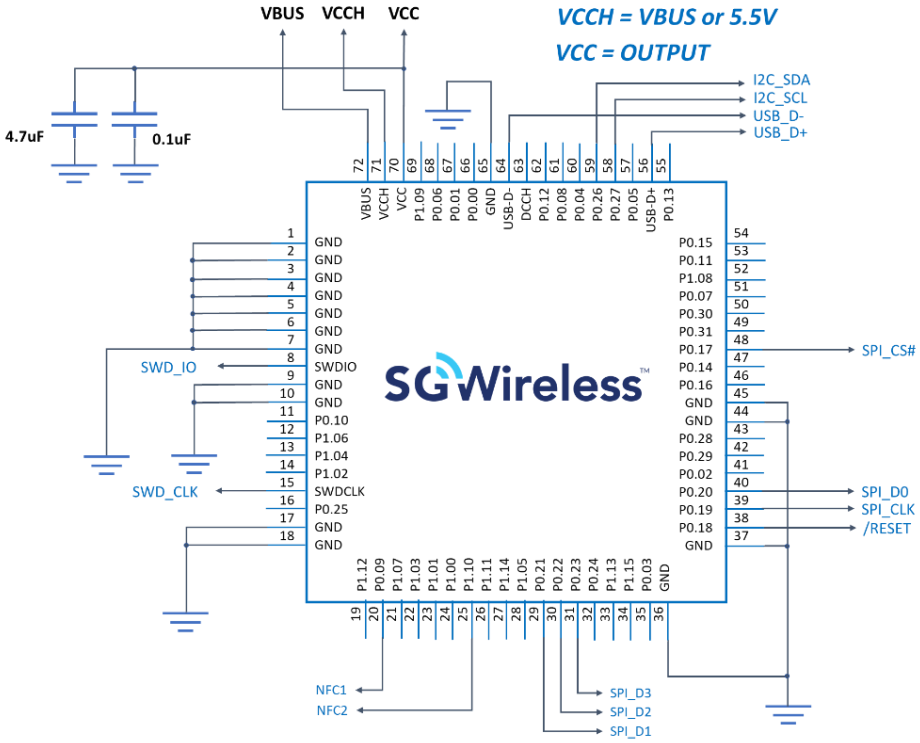


***Figure 2:*** *High Voltage Mode LDO Circuit Configuration*

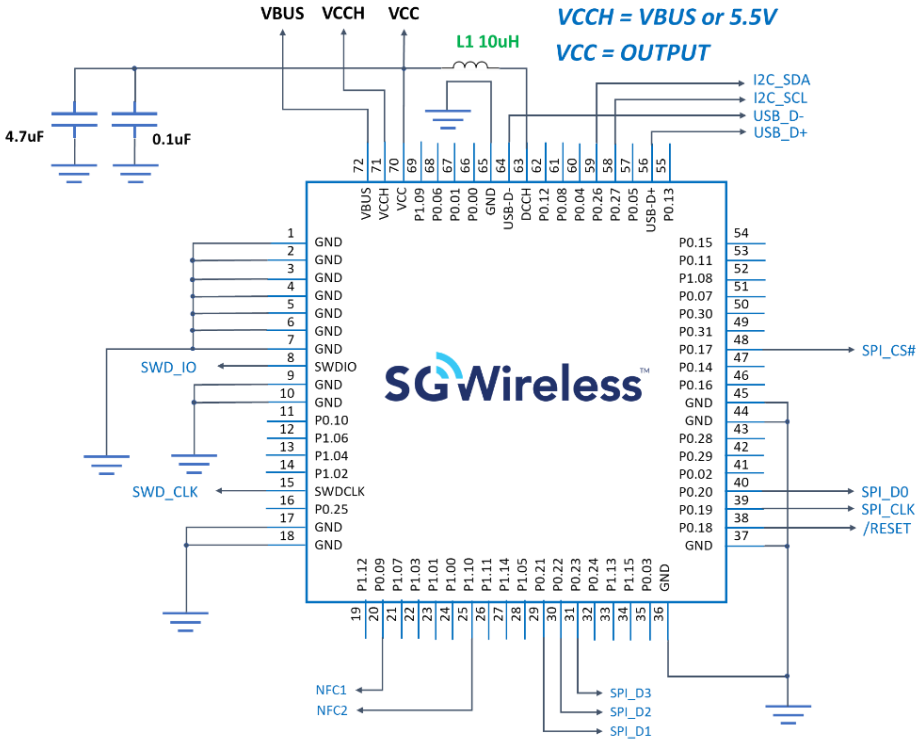


***Figure 3:*** *High Voltage Mode DC/DC Circuit Configuration*

b. Internal DETECT signal, optionally generated by the GPIO peripheral.
The target GPIO pin can be configured to generate the DETECT signal with the SoftDevice function:

```
nrf_gpio_cfg_sense_input(PIN_NUMBER,NRF_GPIO_PIN_PULLUP,NRF_GPIO_PIN_SENSE_LOW)
```

c. Internal ANADETECT signal, optionally generated by the LPCOMP module.
Analog signal function:

```
/** Configures and enables the LPCOMP  */
void LPCOMP_init(void)
{
    /* Enable interrupt on LPCOMP CROSS event */
    NRF_LPCOMP->INTENSET = LPCOMP_INTENSET_CROSS_Msk;

    NVIC_EnableIRQ(LPCOMP_IRQn);

    /* Configure LPCOMP - set input source to AVDD*4/8 */
    NRF_LPCOMP->REFSEL |= (LPCOMP_REFSEL_REFSEL_Ref4_8Vdd << LPCOMP_REFSEL_REFSEL_Pos);
    /* Configure LPCOMP - set reference input source to AIN pin 6, i.e. P0.5 */
    NRF_LPCOMP->PSEL |= (LPCOMP_PSEL_PSEL_AnalogInput6 << LPCOMP_PSEL_PSEL_Pos);

    /* Enable and start the low power comparator */
    NRF_LPCOMP->ENABLE = LPCOMP_ENABLE_ENABLE_Enabled;
    NRF_LPCOMP->TASKS_START = 1;
```

d. Internal SENSE signal, optionally generated by NFC module to wake-up-field.
Function command to enable NFC module:

```
bsp_nfc_sleep_mode_prepare()
```

e. Hardware RESET signal.
The default hardware RESET pin of the Nordic nRF52840 chip set is P0.18. This can be enabled or disabled per Figure 4. Details can be found in the Nordic nRF52840 Datasheet.

The P0.18 reset can be disabled in bootloader by removing the function “Preprocessor Definitions” under “Preprocessor” inside the target project.

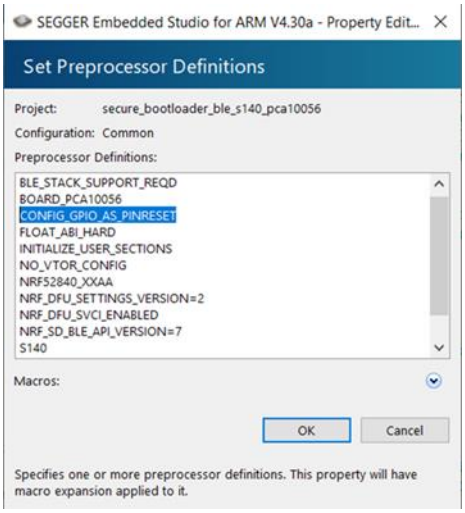


***Figure 4**: Hardware RESET Command*

f. Detecting a valid USB voltage on the VBUS pin.

## Useful Links

1. SG Wireless SGW111X BLE module official product page: https://sgwireless.com/product/SGW111X.
2. Nordic Info Center: https://infocenter.nordicsemi.com/index.jsp.
   All necessary technical files and software development kits for Nordic’s chip.
3. Nordic Developer Zone: https://devzone.nordicsemi.com/questions/.
   Highly recommended for firmware developers. Contains detailed tutorials and allows interaction with other developers and Nordic’s employees to help with any questions.
4. nRF52840 official page: https://www.nordicsemi.com/eng/Products/nRF52840.
   Brief introduction to nRF52840, with download links for Nordic’s developing software and soft devices.

**Revision History**

| Revised | Version | Description |
|---|---|---|
| 13-Mar-2020 | 1.0 | Initial document release |
| 24-Apr-2020 | 1.1 | Circuit diagrams and formatting update |

**Contact us at cs@sgwireless.com for any queries, or find us at any channel below:**

Website: https://sgwireless.com/
LinkedIn: https://www.linkedin.com/company/sgwireless/
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